

Cadence Rtl Compiler Manual

International Conference on Computer Design (ICCD '99)

IEEE Computer Society 1999
The proceedings from the October 1999 conference include 107 technical presentations from 14 different countries. Not restricted to presented papers, this volume includes both the keynote and plenary addresses, poster presentations, as well as the proceedings of two tutorials, one on CAD and one on benchmarking, selecting, and debugging microcontrollers. Topics covered include applied verification techniques, computer arithmetic, intelligent memory, design convergence, test generation and delay testing, microarchitecture, and digital signal processors. No subject index. Annotation copyrighted by Book News, Inc., Portland, OR.

ASIC & EDA 1993

Digital Logic Design Using

Verilog Vaibbhav Taraate

2021-10-31 This second edition focuses on the thought process of digital design and implementation in the context of VLSI and system design. It covers the Verilog 2001 and Verilog 2005 RTL design styles, constructs and the optimization at the RTL and synthesis level. The book also covers the logic synthesis, low power, multiple clock domain design concepts and design performance improvement techniques. The book includes 250 design examples/illustrations and 100 exercise questions. This volume can be used as a core or supplementary text in undergraduate courses on logic design and as a text for professional and vocational coursework. In addition, it will be a hands-on professional reference and a self-study aid for hobbyists.

IEEE VLSI Test Symposium
1999

Transaction-Level Power

Modeling Amr Baher Darwish
2019-08-01 This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

Separation Logic for High-level Synthesis Felix Winterstein
2017-02-27 This book presents novel compiler techniques, which combine a rigorous mathematical framework, novel program analyses and digital hardware design to advance current high-level synthesis tools and extend their scope beyond the industrial 'state of the art'. Implementing computation on customised

digital hardware plays an increasingly important role in the quest for energy-efficient high-performance computing. Field-programmable gate arrays (FPGAs) gain efficiency by encoding the computing task into the chip's physical circuitry and are gaining rapidly increasing importance in the processor market, especially after recent announcements of large-scale deployments in the data centre. This is driving, more than ever, the demand for higher design entry abstraction levels, such as the automatic circuit synthesis from high-level languages (high-level synthesis). The techniques in this book apply formal reasoning to high-level synthesis in the context of demonstrably practical applications. /pp

Reuse Methodology Manual for System-on-a-chip Designs

Michael Keating 1999
Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system

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integration onto a single chip, but also presents significant challenges to the chip designer. As a result, many ASIC developers and silicon vendors are re-examining their design methodologies, searching for ways to make effective use of the huge numbers of gates now available. Design reuse -- the use of pre-designed and pre-verified cores -- is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology. Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry, and to give a

coherent, integrated view of the design process.

EDN 2005

Application Specific Programmable Processor for Sensor Based Networks

Kartik Vaidyanathan 2003

The ASIC Handbook Nigel

Horspool 2001 PLEASE

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INFORMATION PLEASE

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FPGAs for Software

Programmers Dirk Koch

2016-06-17 This book makes

powerful Field Programmable

Gate Array (FPGA) and

reconfigurable technology

accessible to software

engineers by covering different

state-of-the-art high-level

synthesis approaches (e.g.,

OpenCL and several C-to-gates

compilers). It introduces FPGA

technology, its programming

model, and how various

applications can be

implemented on FPGAs without

going through low-level

hardware design phases.

Readers will get a realistic

sense for problems that are

suited for FPGAs and how to

implement them from a

software designer's point of view. The authors demonstrate that FPGAs and their programming model reflect the needs of stream processing problems much better than traditional CPU or GPU architectures, making them well-suited for a wide variety of systems, from embedded systems performing sensor processing to large setups for Big Data number crunching. This book serves as an invaluable tool for software designers and FPGA design engineers who are interested in high design productivity through behavioural synthesis, domain-specific compilation, and FPGA overlays. Introduces FPGA technology to software developers by giving an overview of FPGA programming models and design tools, as well as various application examples; Provides a holistic analysis of the topic and enables developers to tackle the architectural needs for Big Data processing with FPGAs; Explains the reasons for the energy efficiency and performance benefits of FPGA

processing; Provides a user-oriented approach and a sense for where and how to apply FPGA technology.

Proceedings of the ... ACM Great Lakes Symposium on VLSI. 2005

Energy-Efficient Communication Processors

Robert Fasthuber 2013-05-29

This book describes a new design approach for energy-efficient, Domain-Specific Instruction set Processor (DSIP) architectures for the wireless baseband domain. The innovative techniques presented enable co-design of algorithms, architectures and technology, for efficient implementation of the most advanced technologies. To demonstrate the feasibility of the author's design approach, case studies are included for crucial functionality of advanced wireless systems with increased computational performance, flexibility and reusability. Designers using this approach will benefit from reduced development/product costs and greater scalability to future process technology

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nodes.

Low Power Design with High-Level Power

Estimation and Power-

Aware Synthesis Sumit Ahuja

2011-10-22 This book presents novel research techniques, algorithms, methodologies and experimental results for high level power estimation and power aware high-level synthesis. Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC/FPGA design.

17th IEEE VLSI Test

Symposium 1999 The theme of the April 1999 symposium Scaling deeper to submicron: test technology challenges reflects the issues being created by the move toward nanometer technologies. Many creative and novel ideas and approaches to the current and future electronic circuit testing-related problems are explored

Conference Record 1996 Logic and Computer Design

Fundamentals M. Morris Mano 2008 Featuring a strong

emphasis on the fundamentals underlying contemporary logic design using hardware description languages, synthesis, and verification, this book focuses on the ever-evolving applications of basic computer design concepts with strong connections to real-world technology. Treatment of logic design, digital system design, and computer design. Ideal for self-study by engineers and computer scientists.

Northcon/96 1996

IEEE, ACM International Conference on Computer Aided Design International

Conference on Computer Aided Design. Institute of Electrical and Electronics Engineers, 2000, San José, Calif.. 2000 On-Chip Communication

Architectures Sudeep Pasricha 2010-07-28 Over the past decade, system-on-chip (SoC) designs have evolved to address the ever increasing complexity of applications, fueled by the era of digital convergence. Improvements in process technology have effectively shrunk board-level

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components so they can be integrated on a single chip. New on-chip communication architectures have been designed to support all inter-component communication in a SoC design. These communication architecture fabrics have a critical impact on the power consumption, performance, cost and design cycle time of modern SoC designs. As application complexity strains the communication backbone of SoC designs, academic and industrial R&D efforts and dollars are increasingly focused on communication architecture design. On-Chip Communication Architectures is a comprehensive reference on concepts, research and trends in on-chip communication architecture design. It will provide readers with a comprehensive survey, not available elsewhere, of all current standards for on-chip communication architectures. - A definitive guide to on-chip communication architectures, explaining key concepts, surveying research efforts and

predicting future trends - Detailed analysis of all popular standards for on-chip communication architectures - Comprehensive survey of all research on communication architectures, covering a wide range of topics relevant to this area, spanning the past several years, and up to date with the most current research efforts - Future trends that will have a significant impact on research and design of communication architectures over the next several years

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Manual review, we will delve into the intricacies of the platform, exploring its features, content diversity, user interface, and the overall reading experience it promises.

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